An FPGA-Based Advanced Control Strategy of a Grid-Tied PV CHB Inverter

Marino Coppola, Fabio Di Napoli, Pierluigi Guerriero, Diego Iannuzzi, Santolo Daliento, and Andrea Del Pizzo

***Abstract*—In this paper, an advanced control strategy for grid-tied photovoltaic (PV) cascaded H-bridge (CHB) inverter is proposed. The circuit topology consists of a proper number of power cells (H-bridge configuration) connected in series and supplied by individual PV modules. The adopted control method is a mixed staircase-PWM technique performed by means of a sorting algorithm to determine cells' switching state. The cells' state is related to the need of charging or discharging a particular cell much more than the others by calculating the voltage error at each dc-link (e.g., by considering the difference between the maximum power point tracking (MPPT) reference and the measured quantity). A dedicated P&O MPPT permits to control independently the voltage of each dc-link; thus, increasing the power extraction even in mismatched conditions. In order to prove the effectiveness and feasibility of the proposed approach, a set of experiments are performed on a laboratory prototype of a single-phase five-level PV CHB. The control section is implemented on FPGA by using a dSPACE real-time hardware platform; thus, obtaining fully dedicated digital circuits. Experimental results show good performance in terms of MPPT efficiency, total harmonic distortion, and power factor in both normal operation and mismatch conditions.**

***Index Terms*— Grid-tied multilevel converter, photovoltaic (PV) power systems, staircase-PWM modulation.**

NOMENCLATURE

f_{clk}	Main clock frequency of FPGA.
g_j	PWM signal.
h_i	Discrete value of switching state of *i*-th cell.
i_{grid}	Grid current.
i_{in}	Inverter input current.
i_{pvi}	PV current of *i*-th cell.
i_{pvi_f}	Filtered PV current of *i*-th cell.
V_{grid}	Grid voltage.
$\hat{v}_{grid}$	Peak value of grid voltage.
v_{Hi}	Output voltage of *i*-th cell.
v_{inv}	Inverter output voltage.
v_{inv}^{ref}	Inverter output voltage reference.
v_{j_f}	*j*-th element of sorted vector of filtered measured dc voltages.
V_{oc}	Open-circuit voltage of PV panel.
v_{pvi}	PV voltage of *i*-th cell.
v_{pvi}^{ref}	MPPT voltage reference of *i*-th cell.
v_{pvi_f}	Filtered PV voltage of *i*-th cell.
v_{pv_min}	Minimum threshold value of PV voltage reference.
S_{ij}	Switching state of *j*-th power device of *i*-th cell.
Δv_{pvi}	Voltage error of *i*-th cell.
Δv_j	*j*-th element of sorted vector of voltage errors.
T_{MPPT}	MPPT time step.
T_o	Time interval for voltages reading process.
T_{sort}	Sorting algorithm time step.
C_i	DC-link capacitance of *i*-th cell.
K	Modulation region.
L	Inductance of line inductor.
N	Generic number of power cells.

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I. INTRODUCTION

GLOBAL demand for renewable energy continued to rise during the recent years and solar power is achieving higher levels of contribution to clean power generation; thus, assuming a relevant role in matching the electricity demand. In this scenario, one of the main issues is the optimal integration of photovoltaic energy resources in existing electrical distribution systems. As a consequence, the research interest in the area of grid-tied photovoltaic (PV) power conversion systems is growing exponentially. A primary goal of these converters is the increase of the power delivered to the grid by properly tracking the maximum power point (MPP) of the PV panel, by reducing losses and harmonic distortion, while providing high reliability [1], [2].

In order to meet the aforementioned requirements, several power conversion systems have been proposed for interfacing the PV generators to the grid. The four main topologies are [3], [4]: centralized topology, string and multistring topology, ac-module topology. The centralized topology is nowadays considered obsolete, while a growing interest has been shown for string and multistring topology thanks to its enhanced MPPT capability and for the inherently modularity. Nevertheless, the latter topologies usually consist of two power stages: 1) a boost dc-dc converter as front stage to get the sufficient dc-bus voltage and/or to obtain a wider tracking range, and 2) an inverter as second stage to generate the ac utility line voltage. As an alternative to the boost dc-dc converter, a step-transformer can be used to reach the grid voltage. The aforementioned solutions are also used in ac-module topology, but devoted to an individual panel [5], [6]. Distributed dc/ac power conversion is able to remove the mismatch losses among PV modules [3], [7] so resulting in both better MPPT capability and modularity. Unfortunately, the ac-module topology needs high-voltage amplification in order to meet the voltage grid level.

Moreover, as known, in monocrystalline (c-Si) and polycrystalline (poly-Si) solar panels, in normal operating conditions, the MPP position spreads over a range of around 20–30% of the nominal open-circuit voltage, due to irradiation and temperature variations. Unfortunately, in a string under uneven irradiation level, the global MPP could be located out of this range, due to the bypass diodes effect. As a consequence, a wide MPP tracking range is mandatory for string applications. On the other hand, in individual panel applications, the bypass diode effect is absent because each panel is individually controlled. In particular, in [8] and [9], a PV inverter, with individual PV panel power-optimizers [generation control circuits, (GCC)], is proposed in order to obtain the maximum power from each single panel in the string, also under uneven conditions. Moreover, it also shows that the global *P–V* curve always exhibits a single MPP. Consequently, a wide MPPT range is not needed to effectively track the Global MPP.

Thus, the best solution should be able to guarantee the advantages of the ac-module topology in terms of distributed power conversion (i.e., avoiding mismatch losses), while exploiting the possibility of using a single dc/ac power conversion stage, instead of multistage boost topology.

One emerging solution either for high- or medium- voltage transformerless power conversion is represented by multilevel converters as interface for grid-connected PV systems. In particular, the cascaded H-bridge (CHB) configuration represents an attractive solution for the possibility to connect each H-bridge cell to an isolated dc source (e.g., a PV module or a string) [10]–[15]. The main advantages of this circuit topology are the following: 1) a modular structure able to be adapted to different voltage and power levels, thus allowing the sharing of voltage boosting among the cascade (i.e., series) of the H-bridge cells; 2) a multilevel waveform expandable to a number of voltage steps depending on the number of used cells. The increase in the number of voltage levels also allows us to reduce the total harmonic distortion (THD), improving the quality of the output voltages and currents with respect to conventional converters [16]. As a consequence, the output filter requirements become weak in the compliance with the grid harmonics standards [2].

Moreover, the CHB circuit topology permits to control separately the voltage of each dc-link, so improving the MPPT quality. This latter characteristic allows maximizing PV power extraction; thus, increasing the system efficiency also in mismatch conditions.

A drawback is the more complex circuit topology of the CHB inverter; thus, resulting in a more elaborate control strategy. In fact, different H-bridge cells share the same grid current; hence, an unique grid current control loop must be implemented. Moreover, the control method must assure a stable circuit operation even in case of unbalanced conditions due to cells' different temperature and solar radiation [4].

This paper deals with a transformerless operation of the circuit in single-phase configuration and with no need of a dc-dc boost stage. A relevant constraint is represented by the need to perform an overall dc-link voltage higher than grid voltage peak value with the aim of forcing active power from dc sources (PV panels) into the grid. Therefore, the number N of cells and PV modules must be properly chosen in order to meet these requirements. Furthermore, an adequate multilevel modulation technique should be adopted. The favorite choice for PV CHB application is phase shifted pulse width modulation (PS-PWM) as reported in [1], [11]–[14], [17], [18], in [2] both PS-PWM and level-shifted PWM (LS-PWM) are exploited, in [19] a phase-shifted discontinuous pulse width modulation (PS-DPWM) is used to control a three-phase grid-connected system, while in [20] a selective harmonic elimination (SHE) is performed by using an artificial neural network (ANN). By considering a CHB structure with N power cells, the multicarrier modulation techniques (PS-PWM, LS-PWM) need N different triangular carriers properly modified in phase and/or vertical position, so leading to a more complex modulator circuit. It is worth highlighting that PV application requires an unbalanced power distribution among the cells in order to meet the different operating conditions of the PV modules; thus, leading to a PV CHB inverter with unequal dc sources. As a consequence, the previous multicarrier modulation strategies must be properly adapted with the aim of ensuring that each H-bridge cell could handle the power of its corresponding PV generator. In [10], an energy balance controller is used as well as in [2] where additionally rotating carrier approach is performed for LS-PWM in order to achieve desired cells' power balance. In [11], a power controller based on the calculation of available power of each cell is performed, in [14], a voltage balancing strategy based on reactive power control is adopted, while in [13] and [17] a nonactive power control is proposed in order to meet nonactive power demand of a local load while realizing power factor (PF) correction and minimizing distribution losses. Moreover, in [20], SHE method is extended for unequal dc sources by means of nondeterministic approach to solve for the angles; thus, providing dataset to an ANN for real-time application. Instead, the paper proposes a different approach based on mixed staircase-PWM technique [21]–[23] performed by means of a sorting algorithm to determine which cell must be in PWM operation, while the others are in a fixed state in order to obtain the desired multilevel waveform. The proposed modulation is well suited for CHB topology with unequal dc sources and takes advantage of unbalanced power distribution among the cells in order to obtain reduced switching losses and improved converter efficiency. In fact, the multilevel stepped waveform is synthesized with a high-frequency component, corresponding to only one cell per cycle, similar to multicarrier PWM, but with the difference that reduced switching losses are produced [24]. Obviously, the sorting strategy must be properly adapted to the particular application under investigation. As a consequence, the choice of the cells' state is related to the need of charging or discharging a particular cell much more than the others by calculating the voltage error at each dc-link (e.g., by considering the difference between the MPPT reference and the measured quantity). In particular, the cell charging is achieved bypassing the cell itself so resulting in direct connection to the PV panel, which is the only source devoted to charge the power cell (e.g., the grid is not used in order to obtain this result).

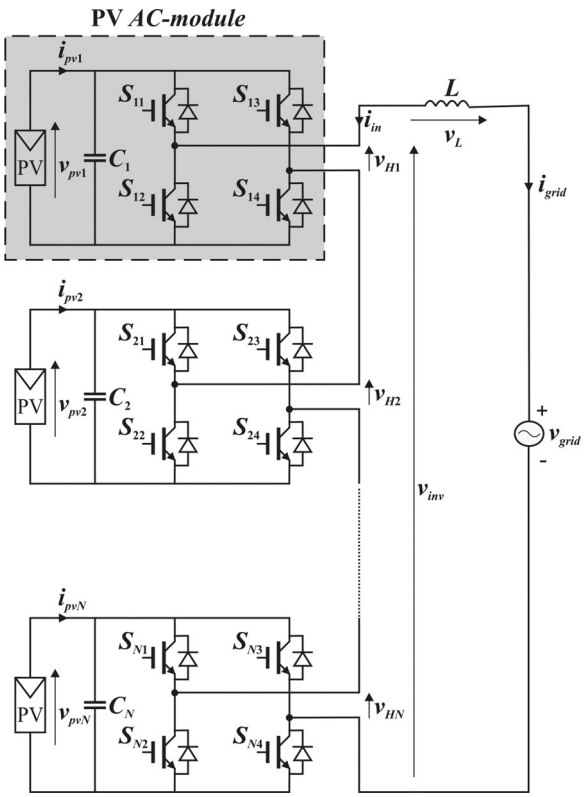

Fig. 1. Single-phase $2N + 1$ level grid-tied PV CHB inverter.

II. System Configuration and Modeling

The grid-tied PV multilevel inverter under study is reported in Fig. 1. Usually, the CHB multilevel converter consists of a generic number *N* of H-bridge cells connected in series. This circuit topology is either useful for string or module connection to the grid. Fig. 1 reports a single-phase $2N + 1$ levels CHB inverter for PV AC-module connection to the grid. Each PV generator is connected to a H-bridge inverter, while the outputs (v_{Hi}) of each H-bridge inverter are connected in series to the grid in order to synthesize the desired ac output waveform (see Fig. 1).

A. CHB Topology Description

The CHB inverter topology provides an output voltage waveform

$$v_{inv} = \sum_{i=1}^{N} v_{Hi}. \tag{1}$$

Depending on the different states of the switching devices, each H-bridge is able to generate three voltage levels as reported in Table I.

As a consequence, the ac output of the inverter is a $2N + 1$ voltage levels waveform. By defining the switch state as a binary signal (i.e., on $= 1$; off $= 0$), the output voltage of each cell can be easily written

$$v_{Hi} = (S_{i1} - S_{i3})v_{pvi} = h_i v_{pvi}, \qquad i = 1, \ldots, N \tag{2}$$

TABLE I
Switching States

State	S_{i1}	S_{i2}	S_{i3}	S_{i4}	v_{Hi}
0	on	off	on	off	0
0	off	on	off	on	0
$+1$	on	off	off	on	$+v_{pvi}$
-1	off	on	on	off	$-v_{pvi}$

where h_i can assume three discrete values: $+1$, -1, 0. Then, replacing h_i with a continuous switching function $\bar{h}_i$ bounded in the interval $[-1, +1]$, the dynamic behavior of the circuit can be described as follows [1]:

$$\begin{aligned} \frac{di_{in}}{dt} &= \frac{v_L}{L} = \frac{v_{grid} - v_{inv}}{L} = \frac{v_{grid} - \sum_{i=1}^{N} \bar{h}_i v_{pvi}}{L} \\ \frac{dv_{pvi}}{dt} &= \frac{1}{C_i}(i_{pvi} + \bar{h}_i i_{in}), \qquad i = 1, \ldots, N \\ i_{grid} &= -i_{in} \end{aligned} \tag{3}$$

where *L* is the inductance of the output filter inductor, while C_i is the capacitance of the dc-link capacitor for power decoupling between the dc source (i.e., PV panel) and the converter. The converter input current i_{in} is in phase opposition with the grid current.

III. Control Strategy

The adopted control strategy aims to reach the following main goals:

1) independent control of each dc-link voltage in order to improve the MPPT quality, so assuring the maximization of PV power extraction also in mismatch conditions;
2) transfer of the overall active power from PV generators to the grid. This result can be first reached by assuring that total dc-link voltage is higher than the grid peak voltage [15]. This condition is also mandatory for a transformerless grid connection. Moreover, the output current i_{in} (see Fig. 1) must be injected to the grid with low harmonic content at unity PF [2];
3) synthesis of a multilevel ac waveform (v_{inv}) at the output of the cascaded converter;
4) stabilization of the converter operation even in the case of unbalanced conditions.

In order to meet the previous requirements, a main inverter control is performed as described in Fig. 2. The outer control loop regulates the overall dc-link voltage to the sum of the references (v_{pvi}^{ref}) given by MPPT algorithm, whose operation will be described in details in the following section. It can be noted that dc voltages are properly filtered (v_{pvi_f}) by using a 100-*Hz* band-stop digital filter in order to avoid the 150-*Hz* harmonic component in the output current (i.e., grid current) [1].

A first PI controller provides the desired amplitude of the converter input current (i.e., the active power which should be transferred to the grid). This amplitude is then multiplied by

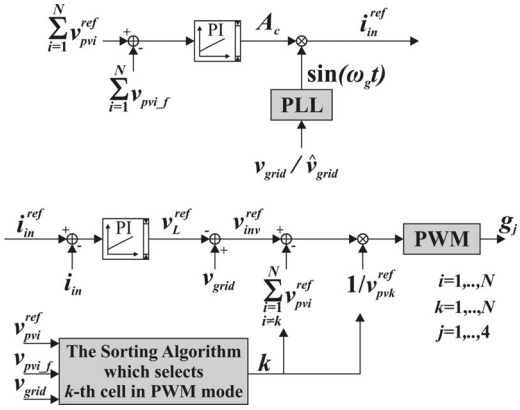

Fig. 2. Control scheme of the PV CHB inverter.

an unity sine wave to derive the current reference. Since the output current (i.e., $i_{grid} = -i_{in}$) must be in phase with the grid voltage, a PLL (Phase Locked Loop) circuit provides the proper sinusoidal waveform.

The inner control loop regulates the current and calculates the voltage reference, which must be subtracted to the grid voltage in order to obtain the ac-side voltage reference of the converter v_{inv}^{ref}. Furthermore, this latter is properly scaled and normalized to form the sinusoidal reference at the input of the PWM modulator. Both the reference quantity to be subtracted from the inverter output voltage reference and the normalization quantity (see Fig. 2) depend on the decision taken by the sorting algorithm as explained in the following sections.

A. MPPT Algorithm

In this paper, a traditional perturb and observe (P&O) MPPT method is used, namely the voltage reference varies (perturb), according to a positive gradient mechanism, while monitoring the power behavior (observe). The algorithm is executed periodically and individually for each cell.

The MPPT input quantities (i.e., PV voltage and current) are digitally filtered to suppress the 100-*Hz* ac fluctuations naturally raising in dc-ac conversion. The filtered quantities v_{pvi_f} and i_{pvi_f} are measured and multiplied to obtain PV power at the given MPPT iteration step. This latter measured power is compared to the power at the previous iteration step in order to carry out the next voltage reference.

The iteration period T_{MPPT} should be large enough to ensure that voltage control loop reaches the imposed voltage reference at every iteration step. In our experiments, the voltage reference step is fixed to 0.5 *V*, while the MPPT time period is equal to 0.1 *s*.

Moreover, the tracking voltage range has a minimum threshold value v_{pv_min}, to guarantee a proper synthesis of ac-side multilevel waveform; it represents the lower boundary of MPP tracking range as well. It is mandatory that the performed voltage range does not include the flat region of the *I–V* curve in order to assure a stable system operation [15].

With the aim of meeting previous requirements, v_{pv_min} is chosen equal to the minimum MPPT voltage by considering the temperature and irradiance range and by taking in mind the nominal ac voltage fluctuations at the dc-link.

TABLE II
SWITCHING STATES

Cell state	S_{i1}	S_{i2}	S_{i3}	S_{i4}	Binary code
0	off	on	off	on	00
$+1$	on	off	off	on	01
-1	off	on	on	off	10
PWM	g_1	g_2	g_3	g_4	11

B. CHB Modulation Strategy

The proposed modulation strategy is a mix of staircase and unipolar PWM.

Each cell of the CHB converter could be in one of the possible four states as reported in Table II.

In the first state the cell is bypassed, while in the second and third states the cell is inserted and its output voltage is fixed to $+v_{pvi}$, $-v_{pvi}$, respectively. In the last state, the cell is properly modulated by using the PWM signals g_j (see Fig. 2).

The proposed technique is generally based on the division of the grid voltage into *N* different regions. It is worth highlighting that the minimum number of cells useful to synthesize the multilevel waveform must be at least equal to the closest integer greater than $\hat{v}_{grid}/v_{pv\_min}$ or rather we can consider the operation in modulation linear region with the aim of defining the minimum dc-link voltage of each cell suitable for this purpose. In particular, in our case, the minimum dc-link voltage v_{pv_min} is imposed by the MPPT as explained in the previous section.

In order to properly synthesize the multilevel waveform, the following steps are needed:

1) identification of the positive or negative half-cycle of the grid sine wave voltage by comparing v_{grid} with zero;
2) calculation of voltage error $\Delta v_{pvi} = v_{pvi}^{ref} - v_{pvi\_f}$;
3) identification of the voltage region *K*.

The proposed sorting algorithm operates at the aim of determining which cell is in PWM mode (state 4 in Table II). The choice of cell state is based on the need to charge or discharge the cell itself in order to guarantee the individual desired tracking of MPP, while assuring stable operation of the system. Fig. 3 shows a flowchart of the sorting algorithm for a generic number *N* of cells. The needed input data are: voltage references (v_{pvi}^{ref}, $i = 1, \ldots, N$) provided by MPPT algorithm; measured dc voltages properly filtered (v_{pvi_f}, $i = 1, \ldots, N$); measured grid voltage (v_{grid}). Then, the algorithm performs the following steps: 1) detection of the positive or negative half-cycle of the grid sine wave voltage; 2) calculation of voltage error ($\Delta v_{pvi} = v_{pvi}^{ref} - v_{pvi\_f}$, $i = 1, \ldots, N$) at dc-link of each cell; 3) sorting of the voltage errors in ascending order ($[\Delta v_1, \ldots, \Delta v_j, \ldots, \Delta v_N]$); 4) mapping for the filtered dc-link voltages derived from sorted vector of voltage errors ($[v_{1\_f}, \ldots, v_{j\_f}, \ldots, v_{N\_f}]$); 5) identification of voltage region *K*, and 6) updating of cells' operating mode. The mapping for the voltage errors in ascending order means that position #*N*

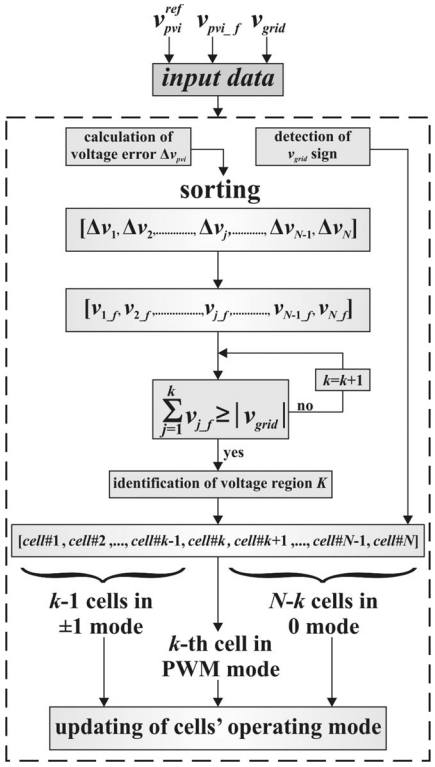

Fig. 3. Flowchart of the sorting algorithm for a generic number *N* of cells. The vector $[\Delta v_1, \Delta v_2, \ldots, \Delta v_N]$ is a mapping of the voltage errors sorted in ascending order.

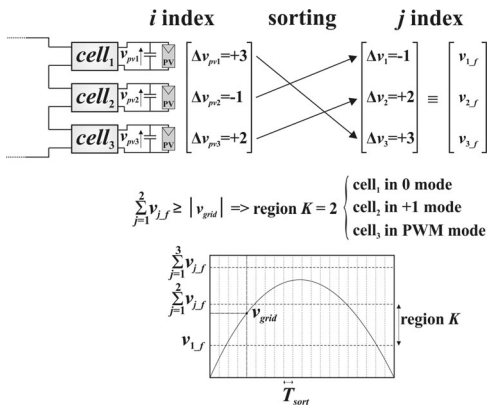

Fig. 4. Sorting algorithm and definition of voltage region *K* in the particular case of $N = 3$.

(related to ordering index *j*, see Fig. 3) corresponds to the cell with the highest positive voltage error (i.e., the cell which must be charged more than the others), while the first vector position corresponds to the cell with the lowest negative voltage error (i.e., the cell which must be discharged more than the others). From the sorted vector of the voltage errors, it can be derived a sorted vector of the filtered dc-link voltages. Then, the identification of voltage region *K* is based on adaptive division of v_{grid} waveform in *N* regions by means of an iterative procedure: when the sum of the sorted dc-link voltages (i.e., v_{j_f}), starting from the first position of the vector, is greater than the measured instantaneous absolute value of v_{grid}, then the voltage region *K* is identified. As a consequence, *k*th cell will be stated in PWM mode, while the first $k-1$ cells of the sorted vector (i.e., the cells with the lower voltage errors) will be in ± 1 mode (discharging mode) and the last $N-k$ cells (i.e., the cells with the higher voltage errors) will be in 0 mode (charging mode). Thus, the output data of sorting algorithm represent the desired cells' operating mode. It is worth highlighting that in all regions the cell charging is related to the need of discharging/charging much more a cell than the others by properly choosing its switching state. In particular, the cell charging is exclusively due to dc sources (i.e., PV panels) with no need of power delivered by the grid. In fact, the proposed approach does not take into account the sign of the input current.

For the sake of clarity, an example with a number of cells $N = 3$ is reported in Fig. 4. By taking in mind that index *i* indicates the cell's position in the physical circuit, as reported in Fig. 1, while index *j* represents the ordering index of the sorted vector, the proposed approach is carefully explained in the following.

The sorting algorithm is executed at every T_{sort} of about 0.1 *ms* (as explained in the following section). At every step of the sorting algorithm, the dc voltages are measured and properly filtered (v_{pvi_f}, $i = 1, 2, 3$). Moreover, the instantaneous value of v_{grid} is measured; thus, also allowing to determine if the grid sine wave is in the positive or negative half-cycle (e.g., in the case of Fig. 4 we have considered the positive half-cycle). By using the references provided by MPPT algorithm, the voltage error ($\Delta v_{pvi} = v_{pvi}^{ref} - v_{pvi\_f}$, $i = 1, 2, 3$) at each dc-link can be calculated; thus, obtaining a first not ordered vector $[\Delta v_{pv1}, \Delta v_{pv2}, \Delta v_{pv3}]$ (see also Fig. 4).

By applying the sorting algorithm to this latter vector, the sorted vector of the voltage errors in ascending order can be obtained $[\Delta v_1, \Delta v_2, \Delta v_3]$. As reported in Fig. 4, the first element Δv_1 of the sorted vector corresponds to the cell with the lowest negative voltage error (in this example, cell_2), while the last element Δv_3 corresponds to the cell with the highest positive voltage error (in this example, cell_1).

Starting from the sorted vector of the voltage errors, a sorted vector of the filtered measured instantaneous dc voltages can be derived $[v_{1\_f}, v_{2\_f}, v_{3\_f}]$, where v_{1_f} corresponds to cell_2 (i.e., is equal to v_{pv2_f}), v_{2_f} corresponds to cell_3 (i.e., is equal to v_{pv3_f}) and v_{3_f} corresponds to cell_1 (i.e., is equal to v_{pv1_f}). Now, the identification of the voltage region *K* can be performed by an adaptive division of the grid waveform in three regions through an iterative procedure: when the sum of the sorted dc-link voltages (i.e., $v_{j\_f}, j = 1, 2, 3$), starting from the first position of the vector, is greater than the measured instantaneous absolute value of v_{grid} (i.e., $\sum_{j=1}^{k} v_{j\_f} \geq |v_{grid}|$), then the voltage region *K* is identified. In the example of Fig. 4, $\sum_{j=1}^{2} v_{j\_f} \geq |v_{grid}|$; thus, the voltage region is $K = 2$ and the cell#2 (*k*th cell) of the sorted vector, corresponding to cell_3 in the physical circuit, will be in PWM mode.

As a consequence, cell_3 will be in PWM mode, while the first $k - 1 = 1$ cells will be in $+1$ mode (in our case it is cell_2 corresponding to first position of the sorted vector) and the

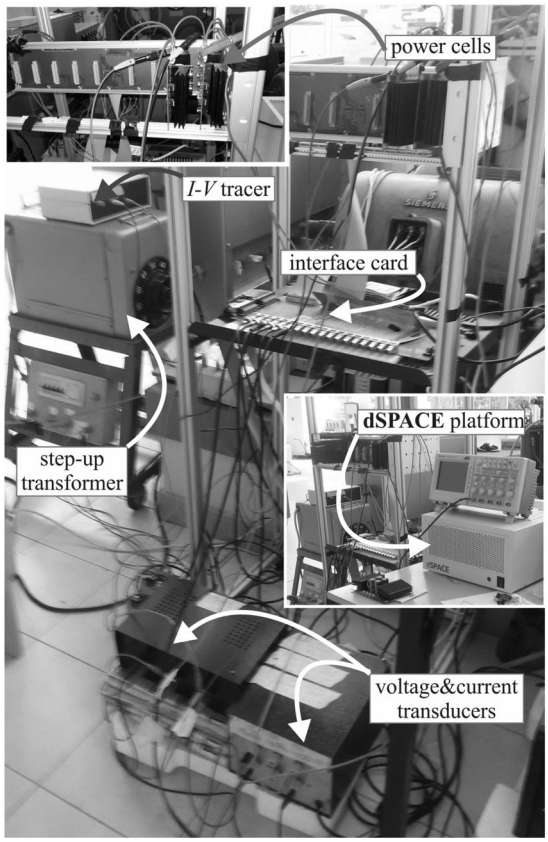

Fig. 5. Laboratory prototype.

last $N-k=1$ cells will be in 0 mode (in our case it is cell_1 corresponding to last position of the sorted vector).

It is worth noting that our purpose is not a voltage balancing among the cells, but stable system operation under unbalanced conditions. The possibility of using the mixed modulation method with unequal dc sources raises from the implementation of the proposed control approach; thus, representing a novelty with regard to [21]–[23]. In fact, the proposed control assures stable circuit operation (also in mismatch conditions), individual tracking of MPP (so maximizing efficiency) and suitable synthesis of the desired voltage waveform with reduced THD at unity power factor.

IV. Experimental Results

In order to experimentally validate the proposed circuit design and control approach, a laboratory prototype of a grid-tied PV modular CHB inverter has been built. It consists of two H-bridges connected in series. Each cell includes one PV module; thus, the available total dc-link voltage is lower than the peak grid voltage (i.e., $230\,V_{rms}$). As a consequence, a transformer has been interposed between the inverter output and the grid at the aim of meeting the grid voltage level.

The test has been conducted by using a real-time hardware platform (dSPACE ds1006) equipped with a field programmable gate array (FPGA) Xilinx Virtex-5 (see Fig. 5). The measurement and control sections are mainly implemented on the FPGA by means of IP blocks from the Xilinx library and of Verilog custom modules in order to obtain fully dedicated digital circuits adapted to the algorithms to implement. Instead, the PI controllers, the PLL circuit, and the PWM block in Fig. 2 are implemented on the processor side of the used platform. The experimental setup is detailed in the following sections.

A. Power Stage

The designed power cell (H-bridge configuration) consists of four IGBT IRGB4056DPbF with a breakdown voltage of 600 *V* and a continuous collector current of 12 *A* at 100 °*C*. The dc-link capacitance is 4.6 *mF* and it is devised to limit the 100-*Hz* voltage fluctuation to about 1 *V* [3]. It is worth noting that a 100-*Hz* oscillation affecting individual dc-link voltages is expected because at steady state the switching behavior of each cell is strongly dependent on the grid voltage.

Each cell is equipped with a resistive divider at the dc-link in order to generate the proper voltage level to put in input to a 12-bit SAR A/D converter (ADS7816), whose digital output is sent to the dSPACE platform with a maximum throughput rate of 200 *kHz* (corresponding to an A/D clock frequency of 3.2 *MHz*). The two cells are inserted in a back-plane (see Fig. 5) equipped with a MUX and DEMUX with the same select lines. The demux input is a signal which enables the voltage measurement of a particular cell based on the selection signals, those also address the corresponding output of the mux, whose inputs are the 12-bit serial data (i.e., digital version of dc-link voltage) of each cell.

The inductance of line filter inductor is $L=5$ *mH*. As aforementioned, the inverter output is connected to the single-phase grid through a transformer. The transformer secondary side exhibits a voltage amplitude of about $27\,V_{rms}$ and a frequency of 50 *Hz* in agreement with the available PV voltage levels.

B. FPGA Control Implementation

The used dSPACE platform (ds1006 equipped with ds5203 and an additional piggy-back module) provides 32 digital I/O, 12 A/D, and 12 D/A channels. The design of the control and measurement sections is obtained by using, in the MATLAB/Simulink environment, XSG (Xilinx System Generator) tool and dSPACE RTI (Real-Time Interface). A simplified schematic view of digital circuits implemented on FPGA is reported in Fig. 6.

The measurement section is devoted to the generation of A/D clock and chip select signals starting from the main FPGA clock ($f_{clk}=1/T_{ck}=100$ *MHz*), in order to allow the reading of the voltages at dc-link of each cell in a time interval $T_0=0.1$ *ms*. A custom Verilog module properly synchronizes the reading process so that it is completed at the end of time T_0 and the read data are available in a bank of registers until the next reading cycle starts.

The duration of the reading period $T_0=0.1$ *ms* accomplishes with the need to have $T_0<T_{sort}$, as shown in Fig. 4. The sorting algorithm, described in Section III-B, is implemented by using Xilinx library blocks and custom Verilog modules in order to obtain the cell state by considering the voltage errors, the corresponding measured filtered voltages, the sign and the absolute

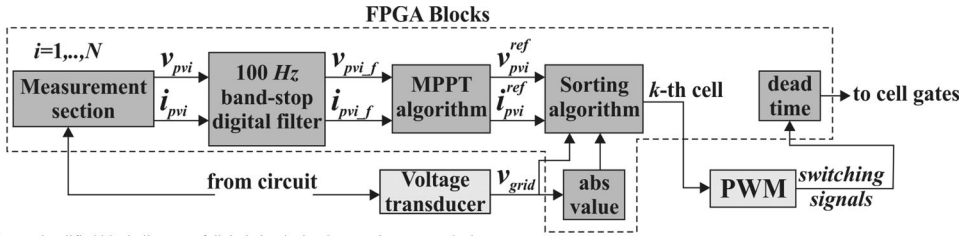

Fig. 6. Simplified block diagram of digital circuits implemented on FPGA device.

value of v_{grid}, the definition of *K* region. This procedure is executed at every $T_0 + 4T_{ck} = T_{sort}$. During this latter period, the cells' state may vary due to change in the voltage errors. The custom Verilog MPPT block performs the algorithm, described in Section III-A, every $T_{MPPT} = 100\ ms$.

As previously explained, the measured PV voltages and currents are filtered before they were sent to the sorting block and also to the MPPT block. The digital filter (100-*Hz* band-stop) is obtained by using a delay line (a chain of registers properly synchronized in order to perform the desired delay). Moreover, the dead-time between the gate signals of the switching devices of the same H-bridge leg is realized by a custom Verilog module on the FPGA.

C. Performance

A wide experimental campaign has been performed in order to verify the effectiveness of the proposed circuit and control design. In the following, for the sake of clarity, two more representative test cases will be investigated. They correspond to normal operation and partial shading conditions, respectively. In the test setup, two commercial PV panels [25] installed on the roof of the Department of Electrical Engineering and Information Technologies in Napoli have been used, instead of the more usual PV simulators (programmable power supplies) as suggested in [26]; a *"home-made" I–V* tracer has been used to collect information about the PV panel instantaneous behavior.

In normal operating conditions ("sunny" case), both the panels have been kept under the same irradiance value (about 700 *W/m*^{2}), while in the partial shading test conditions, panel #1 has been subjected to a partial shadowing obtained by superposing a plastic optical filter on a small part of the three subpanels; thus, reducing the available irradiance down to about 500 *W/m*^{2}. The latter case covers a wide range of architectural shading events (e.g., poles, chimneys, TV antennas, etc.) often affecting small/domestic PV plants.

D. Sunny Case

First, performances have been taken into account in terms of MPP tracking accuracy and efficiency. The individual cell voltage reference v_{pvi}^{ref} is reported during an observation period of 2 *s* for both panel #1 [see Fig. 7(a)] and panel #2 [see Fig. 7(b)]. Moreover, for each panel, the voltage reference is compared to the input voltage v_{pvi} and to the filtered input voltage v_{pvi_f}. As can be observed, the input voltage v_{pvi} has remarkable

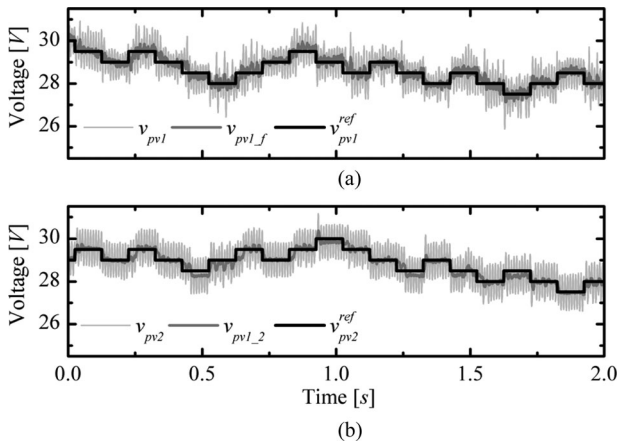

Fig. 7. PV voltage reference v_{pvi}^{ref} (black line) time behavior compared to the measured PV voltage v_{pvi} (light gray line) and to the filtered PV voltage v_{pvi_f} (dark gray line) for the panel #1 (a) and the panel #2 (b), respectively.

100-*Hz* superposed fluctuations due to the dc–ac mechanism, while the filtered signal v_{pvi_f} is not affected by fluctuations proving the effectiveness of the filtering strategy. The voltage reference (black line) has a typical ladder shape due to the P&O MPPT action; in each iteration, the voltage reference changes according to the positive gradient logic. In a steady state, the reference perturbation has a small amplitude and it is quite repetitive around the MPP value; thus, suggesting a suitable control stability. It is worth highlighting that v_{pvi} reaches the reference value stably in every MPPT period. This behavior confirms an appropriate choice of the MPPT frequency with respect to circuit dynamic performance and in particular to dc-link capacitance value.

Fig. 8 reports the position of the operating point for each PV panel superposed to both the *I–V* curves [see Fig. 8(a)] and the corresponding *P–V* curves [see Fig. 8(b)]. The panel characteristics are used as reference in order to better understand the actual position of the operating point of the two panels with respect to the corresponding MPPs.

In particular, the Fig. 8(b) clearly shows that both PV panels achieve an operating point very close to the actual MPP. As a consequence, the overall static MPPT efficiency reaches the noticeable value of 99% over the observation period.

Subsequently, performances were analyzed in terms of PF and THD.

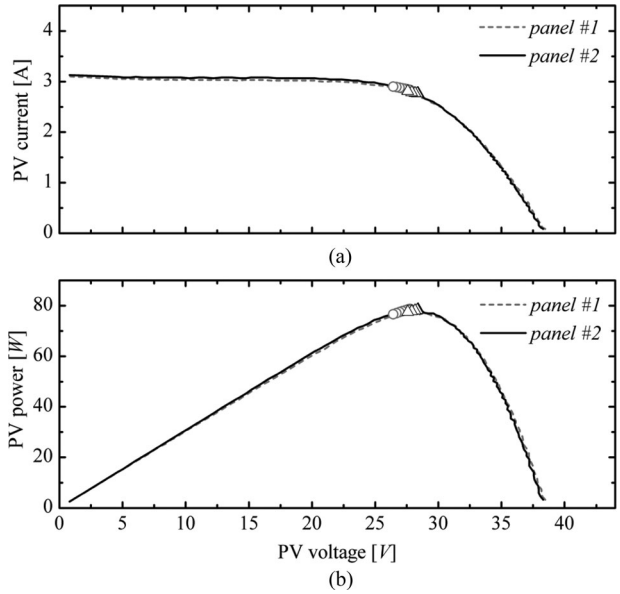

Fig. 8. Sunny case: the operating point position corresponding to panel #1 (circles) and panel #2 (triangles) is highlighted respect to the individual *I–V* curves (a) and *P–V* curves (b) corresponding to panel #1 (dashed line) and #2 (solid line).

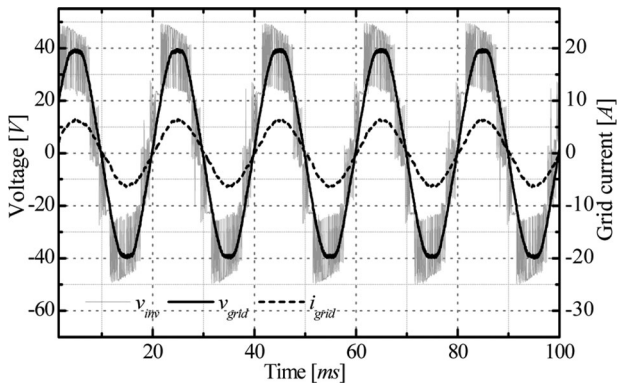

Fig. 9. Output behavior in normal operation: the modulated voltage v_{inv} (gray solid line) is compared to the grid voltage v_{grid} (black solid line). The behavior of the output current i_{grid} (black-dashed line) is also reported.

Fig. 9 compares the multilevel voltage waveform v_{inv} to the grid voltage v_{grid}. The behavior of the output current i_{grid} is also drawn. It is worth noting that v_{inv} suitably synthesizes v_{grid}; thus, proving that the MPPT and the modulation strategy work properly. In other words, in $K = 1$ region both v_{pv1} and v_{pv2} are successfully kept to be greater than the $v_{pv\_\min} > \hat{v}_{grid}/2$, while in $K = 2$ region the sum of v_{pv1} and v_{pv2} remains greater than $\hat{v}_{grid}$. Moreover, the MPPT algorithm forces the operational voltage to be always higher than v_{pv_min}; thus, assuring low current distortion.

The obtained PF (calculated in an integration period equal to a MPPT iteration period) is about 0.995.

Fig. 10 shows the amplitude spectrum of the grid current i_{grid} obtained by performing fast Fourier transform (FFT) analysis over the whole time window. As expected for a multilevel inverter, the amplitude corresponding to the odd upper harmonics are two orders of magnitude lower than the fundamental; thus, allowing the THD value to be rather low, less than 2.5%. The power distribution, normalized with regard to the power of the fundamental harmonic (i.e., 50 *Hz*), is reported in Fig. 11 for the first 40 harmonics.

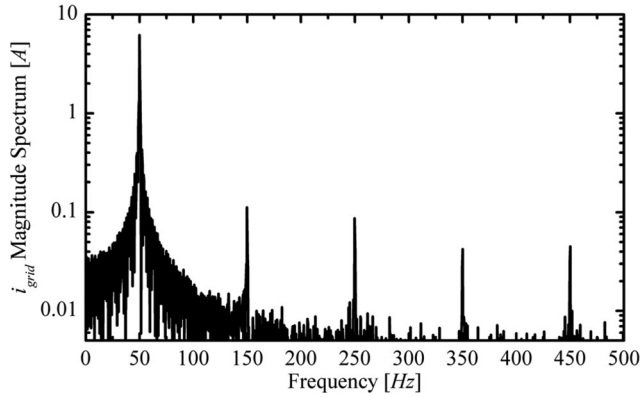

Fig. 10. Magnitude spectrum of grid current obtained by means of FFT calculation over the observation period.

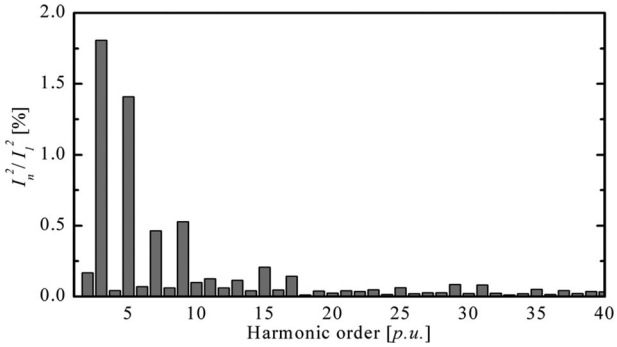

Fig. 11. Power distribution up to the 40th harmonic.

E. Partial Shading Case

In Fig. 12, the MPP tracking behavior is reported in the case of uneven irradiance conditions in order to verify that the MPPT algorithm can individually force the operating point of the panels close to the respective MPPs.

According to the constraints introduced in the Section III, each power cell is able to track a voltage reference in the range $[v_{pv\_min}, V_{oc}]$ independently to the other cells. As a consequence, in case of slight mismatch, the shaded panel does not affect the performance of the overall system because of converter ability to extract the maximum available power from each panel separately.

As already done in Fig. 8, Fig. 13 describes the position of the operating point of each PV panel. The *I–V* curves [see Fig. 13(a)] and the corresponding *P–V* curves [see Fig. 13(b)] are used as reference.

In particular, the Fig. 13(b) clearly shows that both PV panels achieve the corresponding MPPs; thus, converging to different

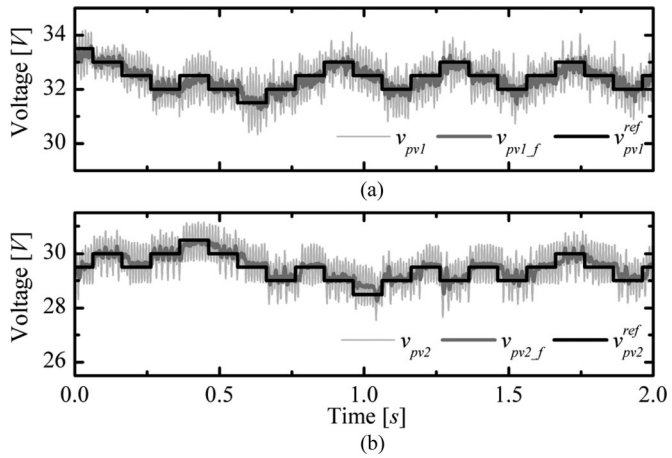

Fig. 12. PV voltage reference v^{ref}_{pvi} (black line) time behavior compared to the measured PV voltage v_{pv} (light gray line) and to the filtered PV voltage v_{pv_f} (dark gray line) for the panel #1 (a) and the panel #2 (b), respectively.

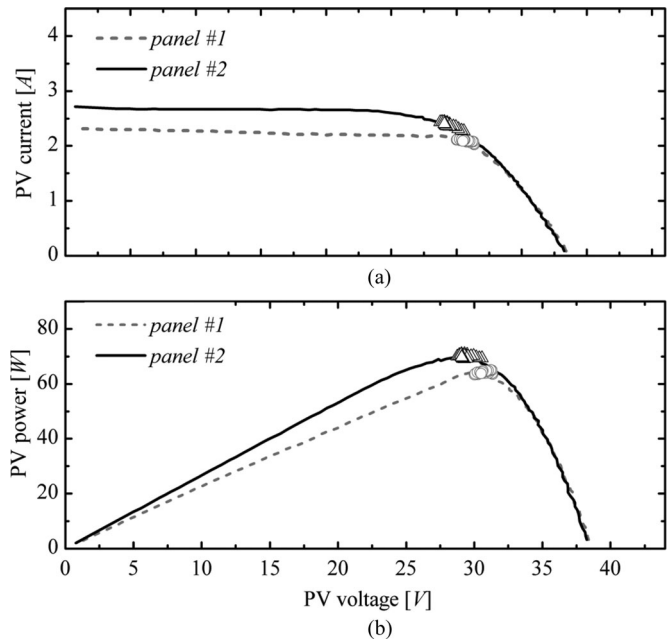

Fig. 13. Partial shading case: the operating point position corresponding to panel #1 (circles) and panel #2 (triangles) is highlighted respect to the individual *I–V* curves (a) and *P–V* curves (b) corresponding to panel #1 (dashed line) and #2 (solid line).

current and voltage levels. As a consequence, the overall static MPPT efficiency is still close to 99.5% over the observation period.

To better quantify the enhancement of the overall efficiency due to the proposed distributed conversion approach, in Fig. 14 the *P–V* curves of the two individual panels are compared with the global *P–V* curve obtained considering the two panels connected in series. The global *P–V* curve takes into account the bypass diodes effect on the shaded panel [27]. In particular, three ideal diodes exhibiting a constant forward voltage of 1 *V* were considered. As expected, the power value corresponding

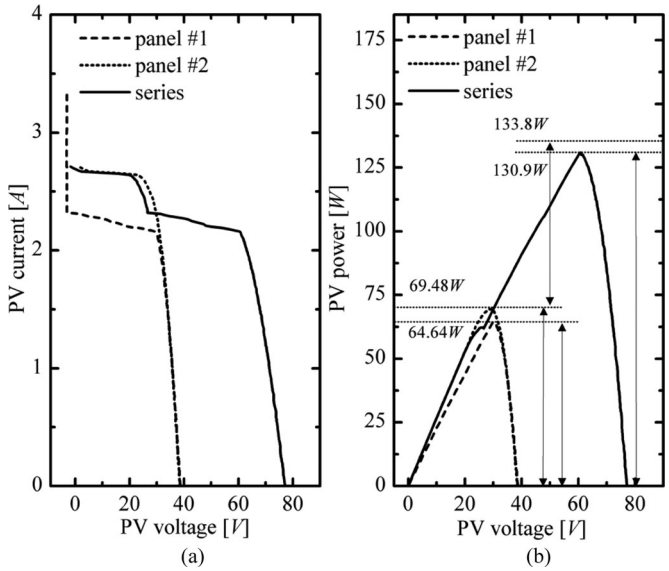

Fig. 14. Concentrated versus distributed convention. In (a), *I–V* curves corresponding to the individual PV panels (#1 dashed line, #2 dotted line) are compared to the curve of the series. In (b), the corresponding *P–V* curves are reported in order to highlight the difference in terms of producible power.

to the global MPP (i.e., 130.9 *W*) in the latter case is lower than the sum of the maximum power (i.e., 133.8 *W*) referring to the panels considered individually. Thus, the proposed approach allows a global power enhancement of about 2%. This low increase accomplishes with the slight shading affecting a reduced number of solar cells in panel #1. It is worth highlighting that in case of deep shading, involving many solar cells, the power enhancement dramatically increases.

V. Conclusion

The paper has focused the attention on the design and control of a grid-tied PV CHB inverter. This converter topology features many advantages such as modularity, high-quality output voltage and current, independent control of each dc-link voltage.

The proposed modulation method based on a mixed staircase-PWM is able to reduce the devices' number in switching mode. This technique is properly adapted to the PV application in order to maximize the power extraction by guaranteeing the individual MPP tracking of each cell through a dedicated sorting algorithm. The proposed control strategy is able to independently regulate the dc-link voltages to MPPT voltage references by means of the used sorting algorithm so increasing the overall system efficiency even in mismatch conditions. Furthermore, the MPPT algorithm has been properly designed in order to assure a stable circuit operation by imposing a lower boundary to the MPP tracking range.

A set of experimental tests have been conducted on the laboratory prototype of a five-level grid-tied PV CHB converter. The obtained experimental results have confirmed the feasibility and the effectiveness of the proposed design and control strategy. In particular, it has been proved that the used MPPT and sorting algorithms allow us to track individually the MPP of each cell

in short time, while assuring a stable operation also in uneven irradiation conditions. The overall static MPPT efficiency has been always greater than 99%.

Moreover, the proposed control technique, including the proper digital filter, has shown the capability of establishing a high-quality injected current with a THD of about 2.5%, while keeping the PF almost unitary.

Further studies will be performed in order to optimize the control strategy at the aim of avoiding the constraint on the fixed minimum value of MPP tracking voltage range. Better results could be obtained by substituting the aforementioned voltage threshold, needed for used P&O algorithm, with an incremental conductance threshold suitable for IC (Incremental Conductance) algorithm; thus, resulting in adaptive MPPT control approach.

REFERENCES

[1] E. Villanueva, P. Correa, J. Rodriguez, M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.

[2] J. Chavarria, D. Biel, F. Guinjoan, C. Meza, J.J. Negroni, "Energy-balance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 98–111, Jan. 2013.

[3] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[4] S. Kouro, B. Wu, A. Moya, E. Villanueva, P. Correa, and J. Rodriguez, "Control of a cascaded H-bridge multilevel converter for grid connection of photovoltaic systems," in *Proc. IEEE 35th Ind. Electron. Conf.*, 2009, pp. 3976–3982.

[5] M. Coppola, S. Daliento, P. Guerriero, D. Lauria, and E. Napoli, "On the design and the control of a coupled-inductors boost dc-ac converter for an individual PV panel," in *Proc. Int. Symp. Power Electron. Electr. Drives Autom. Motion*, Jun. 2012, pp. 1154–1159.

[6] D. Meneses, F. Blaabjerg, O. García, and J. A. Cobos, "Review and comparison of step-up transformerless topologies for photovoltaic AC-module application," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2649–2663, Jun. 2013.

[7] T. K. S. Freddy, N. A. Rahim, H. Wooi-Ping, and H. S. Che, "Comparison and analysis of single-phase transformerless grid-connected PV inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5358–5369, Oct. 2014.

[8] T. Shimizu, M. Hirakata, T. Kamezawa, and H. Watanabe, "Generation control circuit for photovoltaic modules," *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 293–300, May 2001.

[9] T. Shimizu, O. Hashimoto, and G. Kimura, "A novel high-performance utility-interactive photovoltaic inverter system," *IEEE Trans. Power Electron.*, vol. 18, no. 2, pp. 704–711, Mar. 2003.

[10] G. Brando, A. Dannier, and R. Rizzo, "A sensorless control of H-bridge multilevel converter for maximum power point tracking in grid connected photovoltaic systems," in *Proc. Int. Conf. Clean Electr. Power*, May 2007, pp. 789–794.

[11] O. Alonso, P. Sanchis, E. Gubia, and L. Marroyo, "Cascaded H-bridge multilevel converter for grid connected photovoltaic generators with independent maximum power point tracking of each solar array," in *Proc. IEEE 34th Annu. Power Electron. Spec. Conf.*, 2003, pp. 731–735.

[12] J. J. Negroni, F. Guinjoan, C. Meza, D. Biel, and P. Sanchis, "Energy-sampled data modeling of a cascade H-bridge multilevel converter for grid-connected PV systems," in *Proc. 10th IEEE Int. Power Electron. Congr.*, Oct. 2006, pp. 1–6.

[13] B. Xiao, F. Filho, and L. M. Tolbert, "Single-phase cascaded H-bridge multilevel inverter with nonactive power compensation for grid-connected photovoltaic generators," in *Proc. Energy Convers. Congr. Expo.*, 2011, pp. 2733–2737.

[14] M. A. Rezaei, S. Farhangi, and H. Iman-Eini, "Enhancing the reliability of single-phase CHB-based grid-connected photovoltaic energy systems," in *Proc. Power Electron. Drive Syst. Technol. Conf.*, 2011, pp. 117–122.

[15] A. Eskandari, V. Javadian, H. Iman-Eini, and M. Yadollahi, "Stable operation of grid connected cascaded H-Bridge inverter under unbalanced insolation conditions," in *Proc. 3rd Int. Conf. Electr. Power Energy Convers. Syst.*, 2013, pp. 1–6.

[16] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[17] B. Xiao, K. Shen, J. Mei, F. Filho, and L. M. Tolbert, "Control of cascaded H-bridge multilevel inverter with individual MPPT for grid-connected photovoltaic generators," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2012, pp. 3715–3721.

[18] B. Xiao, L. Hang, C. Riley, L. M. Tolbert, and B. Ozpineci, "Three-phase modular cascaded H-bridge multilevel inverter with individual MPPT for grid-connected photovoltaic systems," in *Proc. IEEE 28th Annu. Appl. Power Electron. Conf. Expo.*, 2013, pp. 468–474.

[19] B. Xiao, L. Hang, and L. M. Tolbert, "Control of three-phase cascaded voltage source inverter for grid-connected photovoltaic systems," in *Proc. IEEE 28th Annu. Appl. Power Electron. Conf. Expo.*, 2013, pp. 291–296.

[20] F. Filho, L. M. Tolbert, Y. Cao, and B. Ozpineci, "Real-time selective harmonic minimization for multilevel inverters connected to solar panels using artificial neural network angle generation," *IEEE Trans. Ind. Appl.*, vol. 47, no. 5, pp. 2117–2124, Sep./Oct. 2011.

[21] H. Iman-Eini, J.-L. Schanen, S. Farhangi, and J. Roudet, "A modular strategy for control and voltage balancing of cascaded H-bridge rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2428–2442, Sep. 2008.

[22] H. Sepahvand, L. Jingsheng, M. Ferdowsi, and K. A. Corzine, "Capacitor voltage regulation in single-DC-source cascaded H-bridge multilevel converters using phase-shift modulation," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3619–3626, Sep. 2013.

[23] F.-S. Kang, S.-J. Park, S. E. Cho, C.-U. Kim, and T. Ise, "Multilevel PWM inverters suitable for the use of stand-alone photovoltaic power systems," *IEEE Trans. Energy Convers.*, vol. 20, no. 4, pp. 906–915, Dec. 2005.

[24] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[25] Shell Solar Product Information Sheet, "Shell SQ150-PC photovoltaic solar module."

[26] P. Guerriero, S. Daliento, V. d'Alessandro, and G. Valona, "A simple test-bench to evaluate partial shading effects on the MPPT efficiency of a PV inverter," in *Proc. IEEE Int. Conf. Clean Electr. Power*, 2013, pp. 20–23.

[27] V. d'Alessandro, P. Guerriero, and S. Daliento, "A simple bipolar transistor-based bypass approach for photovoltaic modules," *IEEE J. Photovoltaics*, vol. 4, no. 1, pp. 405–413, Jan. 2014.

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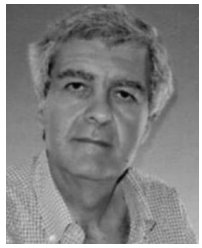

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